This article presents a systematic approach for evaluation and control of logic circuit self-generated noise problems with emphasis placed on the Series 1600 computer system, which utilizes high-speed TTL integrated circuits. Several new techniques are outlined including methods of treating non-linear transmission line terminations and noise summation techniques to insure operation under worst-case conditions.

AN APPROACH TO LOGIC CIRCUIT NOISE PROBLEMS IN COMPUTER DESIGN

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The advent of low nanosecond logic circuits has introduced attendant system noise problems which can cause an otherwise good machine to be useless. Moreover, the problems are constantly being accentuated by an industry trend toward faster circuits. It is important, therefore, to devise a systematic approach for combating this problem.

Once the circuit configurations are fixed, the most important consideration is designing the system interconnection scheme to control the noise problem.

NOISE SOURCES

Let us first examine the different types of noise which may exist in a system and their sources. They may be classified into two categories—externally generated noise and self-generated noise.

Externally generated noise is partially controlled by defining system environmental requirements and providing the logic circuits with as much shielding as possible. This type of noise will not be dealt with further in this article; this article will explore self-generated noise that is produced by various sources within the system.

The major types of self-generated noise are:

1. *Reflections*—noise created by discontinuities in signal lines and end of line termination mismatches;
2. *Crosstalk*—noise created by inductive and capacitive coupling between signal lines;
3. *Power Distribution*—noise created by dc losses, current surges and supply variations.

REFLECTIONS

Line reflections must be considered noise sources when the delay of the line is long compared to the transition time (rise or fall time) of the signal propagating down the line. In short lines the reflections will not be recognized by the receiving circuits. In such cases, precautions against reflections need not be taken unless the reflection amplitude is large enough to cause circuit breakdown.

Long line reflections may have the following effects on the receiver circuits:

1. The circuit may not switch at the proper time;
2. The circuit delay may be increased;
3. The circuit may double switch.

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A rule of thumb for separating long lines from short lines is: If the reflection at the driving end of the line occurs after the transition has been completed, or if it degrades the transition beyond the point where double switching of a receiver could occur, then the line is long. If the reflection occurs during the normal transition time and does not degrade the normal transition beyond the double pulse point, it is a short line. Notice that the short line definition allows some delay increase. The breakpoint in the Series 1600 system between long and short lines was two feet. All lines shorter than this were wired for minimum wire length. For lines over two feet, the wiring was controlled in order to reduce reflection noise. The approach used to derive these controls follows.

End of Line Reflections

The long line reflection noise from an improperly terminated signal line may be quite severe. The reflection coefficient is:

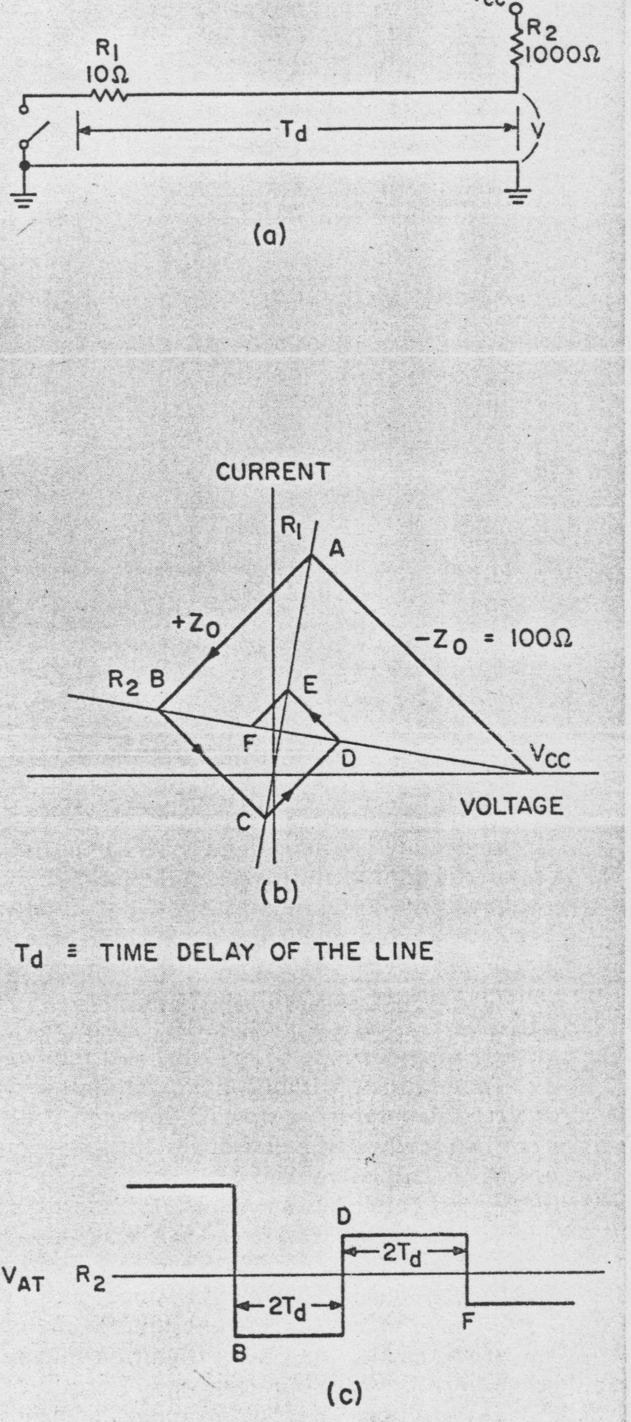
$$\rho = \frac{Z_L - Z_O}{Z_L + Z_O}$$

where Z_L is the impedance of the load and Z_O is the characteristic impedance of the line. For $Z_O = 100\Omega$ and $Z_L = 50\Omega$, the reflection will be one-third the signal swing. When using TTL circuits, the impedance at the end of the signal line is often capacitive with a non-linear resistive element. Both of these factors must be considered in the analysis. The method of calculating reflections from lumped capacity is treated later, while a simplified method for analyzing non-linear load impedances is presented here.[1] To illustrate the method, first consider a linear resistance termination (Fig. 1).

The lines R_1 and R_2 are the impedances at the ends of the line. Starting at V_{cc} (the initial state of the line) a line is drawn with a slope of $-Z_O$ until it intersects R_1. Point A is the current and voltage condition at R_1 immediately after the switch is closed. From point A, a line is drawn with a slope of $+Z_O$ until it intersects R_2. Point B is the current and voltage condition at R_2 after the voltage change from V_{cc} to O V and current change from O to $\frac{V_{cc}}{Z_O}$ have traveled to R_2. This is a negative undershoot. The process is continued and point D is the first positive overshoot, after the reflection has traveled back to the source (point C) and been re-reflected to the load. This is the noise that could cause a circuit to switch, if it exceeded the noise immunity.

Line attenuation at high frequencies rounds off the corners, but is not normally a significant factor in determining the waveform amplitudes.

The graphical method may now be applied to non-linear terminating impedances such as TTL exhibits. The dc input and output impedance curves may be obtained by measurement with a transistor curve



Td ≡ TIME DELAY OF THE LINE

Fig. 1 Method of calculating reflections for a linear resistive termination: a) linear termination; b) graphical method of interpreting the reflections; c) resulting waveform with resistive termination.

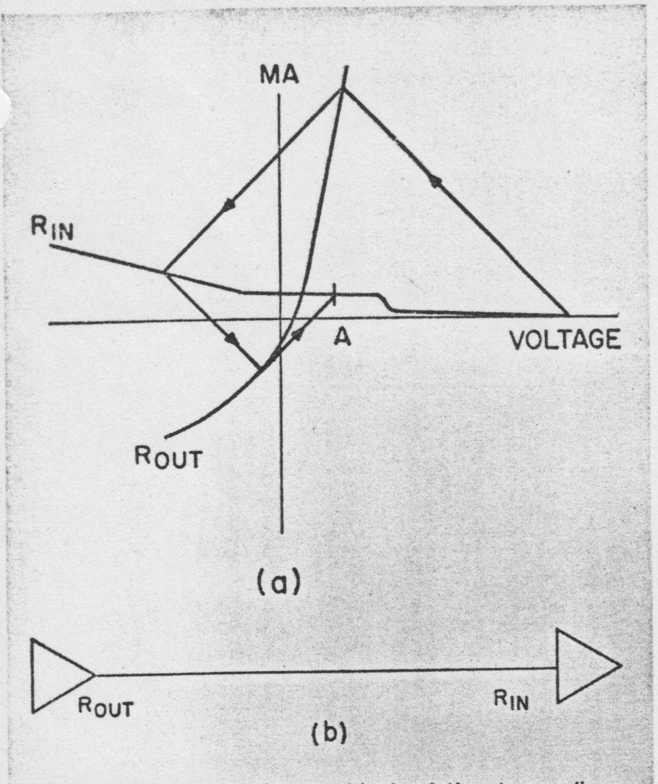


Fig. 2 Application of the graphical solution to non-linear terminations.

tracer and are shown in Fig. 2. The voltage at point A the first positive overshoot and is the noise of concern.

The advantages of this method now become apparent.

1. The parameters which determined the reflection are immediately obvious and may be controlled by specification. In this case they are the dc resistance of both the input (R_{in}) and output (R_{out}) at negative current and voltage levels. These parameters vary greatly from vendor to vendor and are not normally specified.
2. The effects of altering R_{in} and R_{out} by various loading methods may be analyzed and the worst-cases determined without time consuming trial and error laboratory setups. For instance, if there were two loads at the end of the line R_{in} would be cut in half as in Fig. 3A, and the reflection reduced. Therefore, one load is the worst-case. However, if there were added loads at the source, then R_{out} would change as shown in Fig. 3B, and the reflection would be worse. Thus, the worst-case is many loads at the source, but only one at the end of the line, a condition that may not be obvious without the graph.
3. Other conditions may be investigated such as various line impedances and load locations.
4. This method may also be applied to a line switching from a low to high signal level.
5. Any circuit configuration may be used.

Distributed Load Reflections

Distributed loads with capacitive inputs can change the impedance of a transmission line and cause line

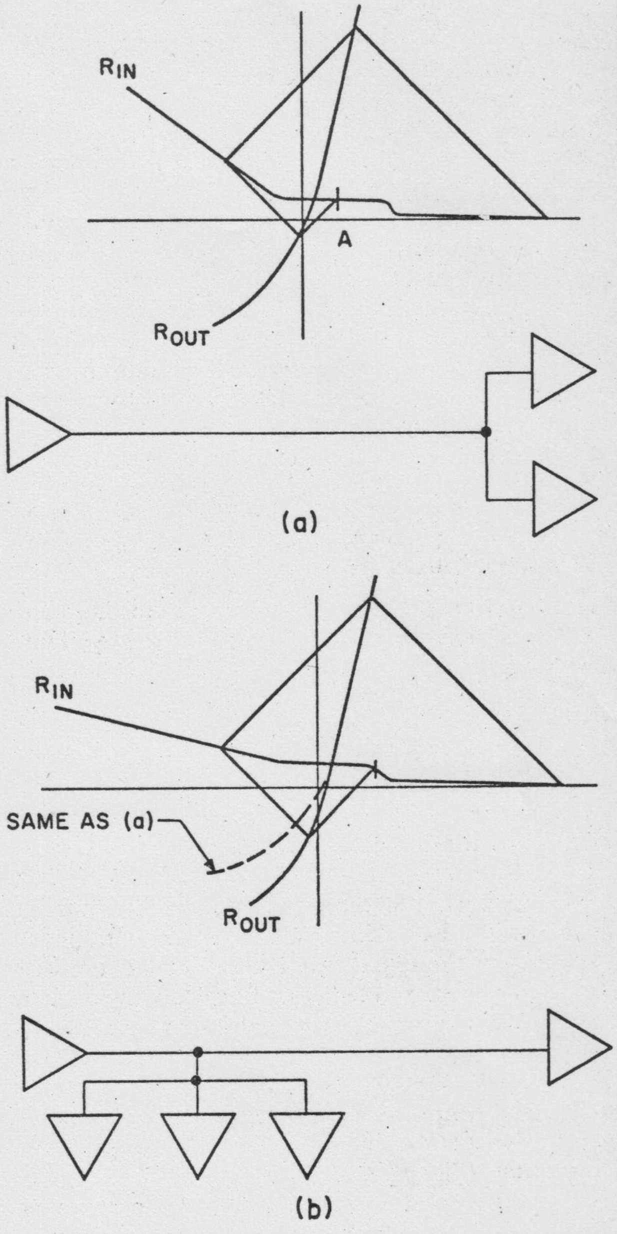
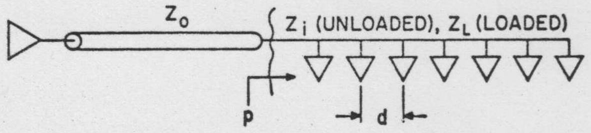


Fig. 3 Variations in the reflections due to a) two loads at the end of the line or b) additional loads at the source.



DEFINITION OF TERMS:

Zi = INTRINSIC IMPEDANCE OF LOADED SECTION.
ZL = LOADED IMPEDANCE OF LOADED SECTION OF LINE.
Zo = DRIVING LINE IMPEDANCE.
Ti = UNLOADED DELAY OF LOADED SECTION.
Cin = INPUT CAPACITANCE OF CIRCUITS.
Rin = INPUT RESISTANCE OF CIRCUITS.
ρ = REFLECTION COEFFICIENT BETWEEN DRIVING LINE & LOADED SECTION.
d = SPACING BETWEEN LOADS.
C = INTRINSIC CAPACITANCE PER UNIT LENGTH OF Zi.
L = INTRINSIC INDUCTANCE PER UNIT LENGTH OF Zi.

Fig. 4 Impedance may be controlled by restricting the spacing, d, between loads.

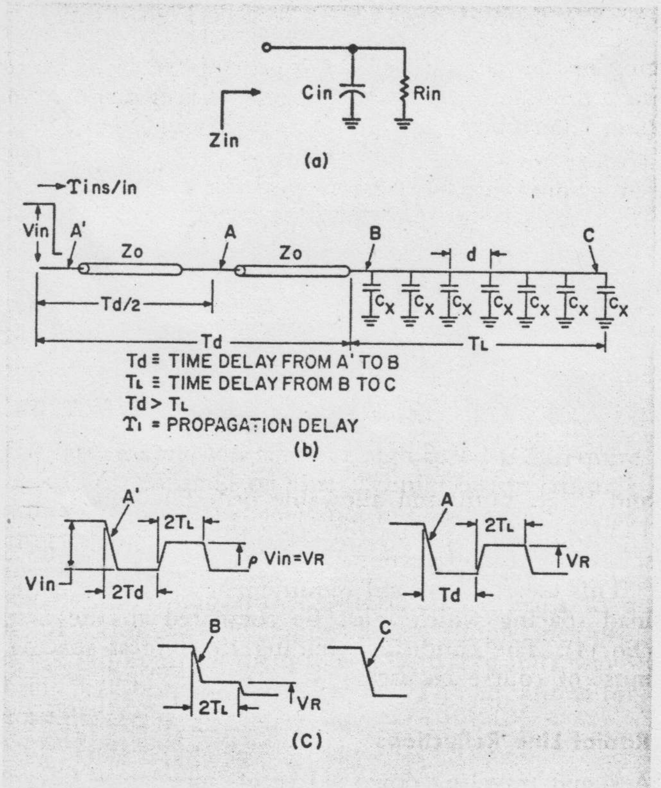


Fig. 5 Analysis of the loading arrangement of Fig. 4: a) load input representation for input signals in transition; b) simplified circuit based on C Z; c) resulting line reflections.

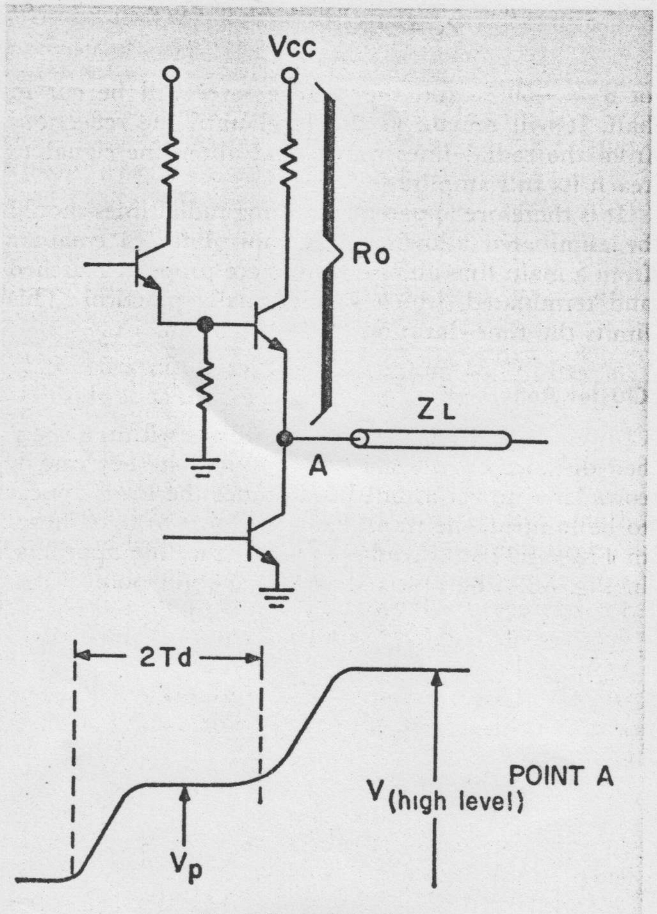


Fig. 6 Pedestal effect.

mismatches. Therefore, it is not sufficient to match line segments to their intrinsic impedances, but rather to a range of line impedances that vary with loading. The range of impedance may be controlled by restricting the spacing between loads.

Consider the case shown in Fig. 4. When the input signal is in transition, the load inputs may be represented as in Fig. 5A. This input impedance is approximated by an effective input capacitance (C_x), which is the capacitance which produces the same reflection as the circuit. The transmission line then reduces to that shown in Fig. 5B and the reflections along the line are shown in Fig. 5C. The spacing between the loads must be adjusted to insure that the loaded impedance (Z_L) is not decreased to the point where the mismatch with Z_O will cause a significant reflection.

The following equations (high frequency approximations) determine the minimum spacing (see Figs. 4 and 5):

$$Z_i = \sqrt{\frac{L_i}{C_i}} \tag{1}$$

$$Z_L = \sqrt{\frac{L_i}{C_i + \frac{C_x}{d}}} \tag{2}$$

$$\rho = \frac{Z_L - Z_O}{Z_L + Z_O} \tag{3}$$

Solving for the minimum spacing yields:

$$d_{min} = \frac{C_x Z_O^2}{\begin{matrix}\tau_i Z_p\\ Z_i\end{matrix}} \left[\frac{1}{\left(\frac{1-\rho}{1+\rho}\right)^2 - \left(\frac{Z_O}{Z_i}\right)^2} \right] \tag{4}$$

All of these parameters are determined by the circuit and its environment, except ρ which is the reflection coefficient for the maximum allowable noise.

The reflection due to the non-linear resistive element of the input adds to the capacitive reflection and should be taken into account when the number of loads becomes large. This may be done by reducing the maximum allowable reflection coefficient.

Pedestal Reflection

The rise time of a TTL circuit is a function of the load impedance and the source output resistance of the output stage. For very short lines, the voltage will rise directly to the high level. For long lines the voltage at the output will rise to a level approximated by the voltage divider of the impedance of the transmission line and the source output resistance. This is much lower than the normal high-level. The output will remain at this level until the reflection from the end of the line returns and brings the output to a full high-level. Therefore, TTL circuits depend on the reflection from the end of the line to bring the output to the full high level. This we call the pedestal effect (Fig. 6).

The impedance (Z_L) can be controlled to insure that the pedestal level occurs above the threshold re-

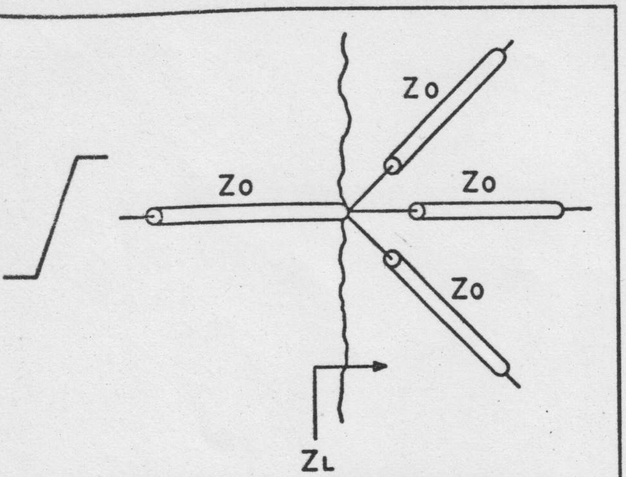


Fig. 7 Transmission line split described by Eq. 6.

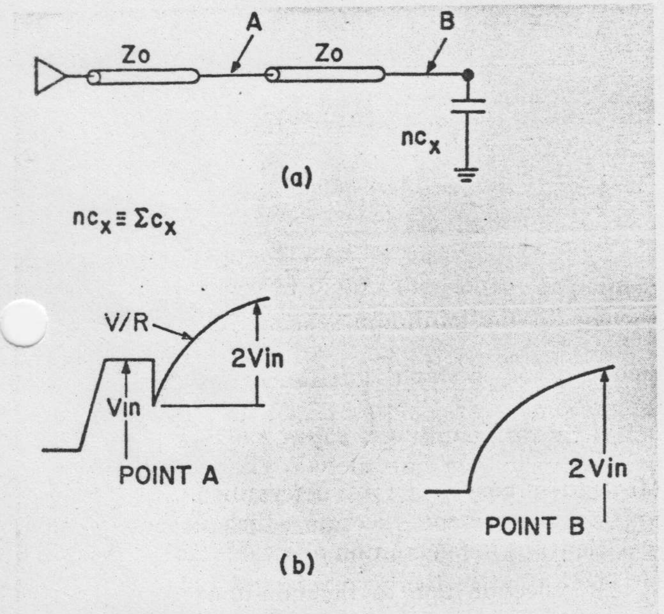


Fig. 8 Equivalent transmission line for an end-of-line cluster; b) waveshapes along the line.

$$V_{IN} = \begin{cases} Kt, & t \leq t_1 \\ Kt_1, & t > t_1 \end{cases}$$

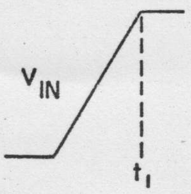


Fig. 9 Input ramp function.

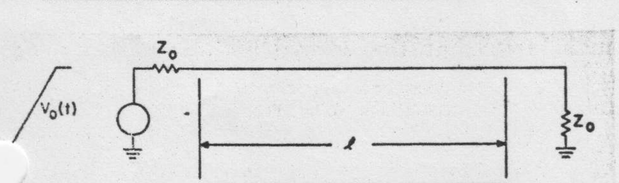


Fig. 10 Evaluation of crosstalk waveforms.

gion of the receivers. This is accomplished by specifying a minimum spacing *d* between loads on the driven line. The required minimum spacing is:

$$d_{min} = \frac{C_x}{\tau_i Z_O \left(\frac{1}{Z_L^2} - \frac{1}{Z_i^2}\right)} \quad (5)$$

where the minimum value of Z_L is approximated by,

$$Z_L = \frac{V_p \quad \overline{R_O}}{\underline{V_{cc}} - \underline{V_p}}$$

and V_p = minimum allowable pedestal level. (This equation is the worst-case since it neglects the small initial load currents).

This creates a second requirement for a minimum load spacing which must be compared to the first (Eq. 4). The condition yielding the largest spacing must of course be used.

Radial Line Reflections

A signal traveling down a line of impedance Z_O can create a severe reflection when it drives more than one line of the same impedance. In the example shown in Fig. 7,

$$\rho = \frac{Z_L - Z_O}{Z_L + Z_O} \text{ where } Z_L = Z_O/3 \quad (6)$$

or $\rho = -50\%$, and the voltage level will be cut in half. It will remain at this level until the reflections from the radial lines return and allow the signal to reach its full amplitude.

It is therefore apparent that long radial lines should be eliminated allowing only short lines to emanate from a main line unless all lines are properly matched and terminated, which is not usually practical. This limits the time duration of the reflection.

Cluster Reflections

Clusters are defined as a group of loads within a specified distance on the main line such that they can be considered to act at one point. Since the loads appear to be lumped, the transmission reduces to that shown in Fig. 8A. The waveshapes along the line appear as in Fig. 8B. The reflected voltage V_R (at point A) is:

$$V_R = K\left[t - 2 Z_O NC_x (1 - \exp[-t/Z_O NC_x])\right]$$

$$0 < t \leq t_1$$

$$V_R = K\left[t_1 - 2 Z_O NC_x \left(\exp\left[\frac{-(t - t_1)}{Z_O NC_x}\right] - \exp[-t/Z_O NC_x]\right)\right] t > t_1 \quad (7)$$

where K is the slope of the input ramp function described in Fig. 9.

The voltage anywhere along the line is $V_{IN}^{(t)} + \rho\, V_{IN}^{(t)}$.

The reflection can become severe as the number of loads increases. These equations neglect the effect of the non-linear resistive element since this is accounted for by the graphical method. In this case the resistive element determines the reflection amplitude after the initial and much larger capacitive reflection.

CROSSTALK

The fast rise and fall times of high speed IC's require the use of transmission line techniques for crosstalk evaluation. Mutual capacitance and inductance calculations using lumped parameters are no longer valid since crosstalk waveforms differ at each end of the line. Transmission line crosstalk theory leads to a useful technique.[2] By taking a few simple measurements and applying them to constants, crosstalk waveforms may be predicted (Fig. 10). The equations for crosstalk are:

$$V_B(t) = K_B\left(\frac{2T_d\,V_O}{T_R}\right),\ T_R > 2T_d \qquad (8)$$

$$= K_B\,V_O,\ T_R < 2T_d$$

$$V_F(t) = K_F\, d\,\frac{V_O(t)}{dt} \qquad (9)$$

thus,

$$K_B = \frac{V_B}{V_O},\ T_R < 2T_d \qquad (10a)$$

and

$$K_F = \frac{V_{F\ max}}{l\left.\frac{dV_O}{dt}\right|_{max}} \qquad (10b)$$

The backward crosstalk waveform $V_B^{(t)}$, has an amplitude that is independent of the transition time (T_R) and line length when $T_R < 2T_d$ and has a width of $2T_d$, where T_d is the propagation delay of the line. The forward crosstalk waveform $V_F^{(t)}$ has an amplitude dependent upon the transition time and length of line and has a width equal to the transition time.

Once the constants K_B and K_F are determined for the coupling of interest, the crosstalk waveforms for various lengths, transition times or signal swings may be calculated. These constants are easily measured whereas the normal method of measuring or calculating mutual capacitance and inductance is difficult and frequently inaccurate. One measurement of V_B, V_F, V_O and the transition time determines K_B and K_F by Eq. 10a and 10b. This measurement may be made at any reasonable V_O and transition time for the coupling of interest. The reflections of crosstalk waveforms from the end of the line terminations may be treated by the graphical method presented earlier.

POWER DISTRIBUTION NOISE

The design of the power distribution system of a computer has frequently been one of trial and error. The analysis of the noise generated involves cumbersome impedance equations for various geometries of conductors. These tended to discourage theoretical calculations and make decisions regarding trade-offs between lower impedance versus more stored charge difficult.

For this design the impedance equations were programmed on a computer. The output of the computer consisted of the following impedance parameters versus any variable of interest:

1. L_{INT} = the internal inductance of the conductor due to current concentration near the periphery of the conductor.
2. L_{EXT} = the inductance due to the proximity of the return path.
3. R_{dc} = the dc resistance.
4. R_S = the resistance due to the skin effect.
5. C_{EQ} = the equivalent capacitance including dielectric losses due to frequency.

The noise generated on the power and ground lines is determined by these parameters in the following equation:

$$\Delta V \approx I_{dc}\,R_{dc} + \left(\frac{1}{2}\sqrt{\frac{L_{INT} + L_{EXT}}{C_{EQ\ (LINE)} + C_{EQ\ (CAPS)}}} + R_S + R_{dc}\right)\Delta I \qquad (11)$$

The first term is the dc loss due to the constant current flowing through the dc resistance of the buss. The second term is the voltage change due to the current pulse caused by the switching circuits of the plug-in.

The current pulse is caused by the difference in dc currents of the two logic states, plus the current to charge or discharge circuit and signal line capacitance, plus the current surge flowing while both the upper and lower transistors of the TTL output are on. The rise and fall time of the current pulse determines the frequency to use for the impedance calculations.

The equation is then applied in successive steps, i.e., from the plug-in to the backplane, until the power supply is reached.

The impedances in the noise equation are plotted as a function of the variables of interest (such as frequency, width of conductors, spacing between planes). Then, the various trade-offs between quantity and location of capacitors, types of busses and/or planes are made to arrive at the noise level.

CIRCUIT NOISE IMMUNITY

System noise must be controlled to insure that the summation of all the above noise is not greater than the level the circuit can tolerate. This level may be found theoretically, empirically or by a combination

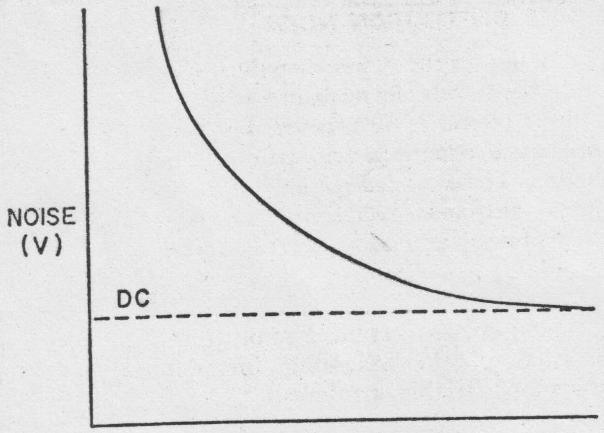


Fig. 11 Typical noise immunity curve.

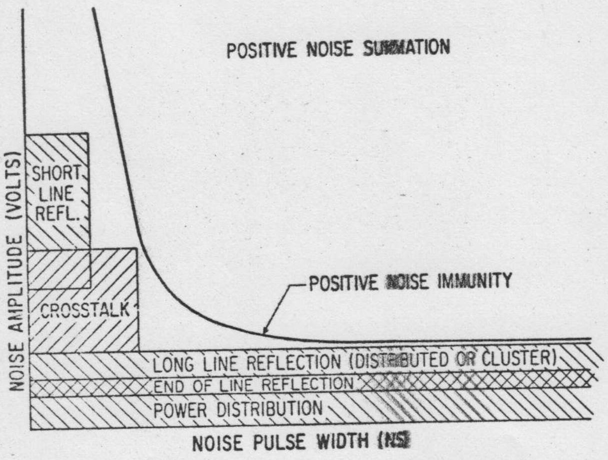


Fig. 12a Positive noise summation.

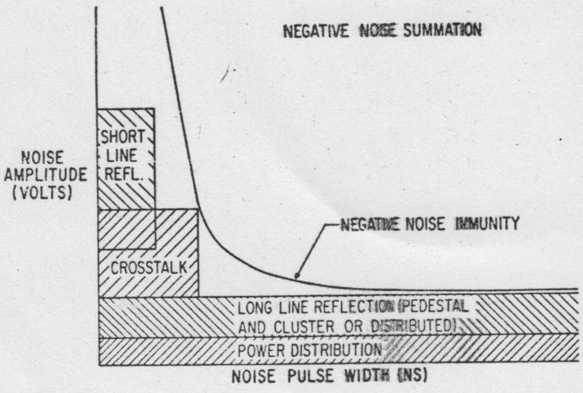


Fig. 12b Negative noise summation.

of both. A typical noise immunity curve appears in Fig. 11.

The tolerable level of noise is defined here as the level of noise at the input of a chain of worst-case gates that will create a noise pulse of an equal level at the output of the chain. This is known as the unity gain concept of noise immunity. It is simply a measure of the maximum noise that, introduced at the input of the chain of circuits, will die out in the system. A noise pulse of greater amplitude may become amplified as it propagates through the system, thus creating a false signal which could be remembered by a flip-flop, one-shot or other storage and edge triggered devices.

CONTROLLING NOISE

We have thus far defined the problem, listed the noise sources, and determined the expressions which dictate the amount of noise to expect. Many variables in the expressions are determined by the package and circuits. The problem now is to assign values to the remaining variables such that the summation of all worst-case noises is less than the noise immunity of the chain of worst-chain circuits. It should be noted that other design philosophies may be used. For instance, only a percentage of each noise may be considered to act at any one time or each noise may be individually compared to the noise immunity curves. These are not worst-case conditions and involve various degrees of risk.

TABLE I—Variables for All Noise Sources

NOISE	VARIABLES
End of Line Reflection	1. Line Impedance (Z_1) 2. Circuit Input & Output Impedance
Distributed Load Reflc.	1. Spacing Between Loads (d) 2. Line Impedance (Z_1)
Pedestal Reflection (Negative Noise Only)	1. Line Impedance (Z_1) 2. Spacing Between Loads (d)
Cluster Reflection	1. Number of Loads (N) 2. Line Impedance (Z_o)
Radial Line Reflection	Length of Lines
Crosstalk	1. Type of Line 2. Line Spacing 3. Parallel Line Length
Power Distribution Noise	1. Impedance of Current Path 2. Filter Capacitance

The summation process is now carried out for positive and negative noise immunity curves as shown in Fig. 12. This presents various trade-offs to be considered by the designer. The power distribution noise for example may be increased at the expense of reflection noise. More crosstalk may be allowed if reflections or distribution noises are reduced, etc. Notice also that the noise generated must be controlled to satisfy the worst of the positive or negative noise immunity curves. Once the trade-offs have been made, usually through several iterations, the final summation is complete.

The power distribution noise which can last for a long ac time period is controlled to the desired level by adjusting the impedance and filter capacitance of the system for a given plug-in and backplane geometry.

The long line reflections (either pedestal, or distributed) also may last for long ac periods compared to the circuit noise immunity curves. They are controlled by choosing the proper value of minimum spacing and type of line. Their amplitude may bring the partial summation to a value just below the dc noise immunity of the circuits. The proper value of minimum spacing is the larger of the two derived from Eq. 4 or 5. Note that the pedestal reflection occurs only on the negative noise immunity curves.

Crosstalk amplitude and width are adjusted to guarantee not to break through the curve. They are controlled by specifying the maximum allowable parallelism length for a given type and number of lines, assuming they are tightly bundled.

The end of line reflections are adjusted by controlling the circuit input impedance. For the Series 1600 system, the graphical method was used. It was found that under worst-case conditions the reflections would exceed the noise immunity curves. Therefore, the circuit parameters required altering. The input impedance of TTL showed that there was a reverse diode connected to the substrate (Fig. 13). This diode had a high resistance and varies from vendor to vendor and from lot to lot. Improving the diode characteristics significantly reduced the reflection and made it nearly independent of loading and Z_0. As shown in Fig. 13, the reflection was reduced from B to B′. The TTL vendors were shown the value of improving the substrate diode or adding an improved diode to each input. A test for the desired characteristic was added to the purchase specification and each vendor altered his basic line of TTL. Thus, end of line reflections were essentially eliminated as a noise problem and no wiring restrictions or line terminations are required for this noise source. The small reflection that can occur may last for long ac time periods, but its amplitude is not sufficient to break the curve when added to power distribution noise. It cannot add to the long line reflections since it cannot occur at the same time. This reflection occurs only on the positive noise immunity curves.

The reflection caused by a cluster is covered by the reflection block in Fig. 12 until the number of loads in the cluster becomes large enough to cause the reflection to break through the curve. In this case, the reflection can be controlled to a certain extent by the line impedance, but usually not to a level which is acceptable to the system. It is therefore, necessary to avoid this reflection by prohibiting the placement of loads in front of the cluster. As a result, the cluster reflection does not appear in the summation of noises.

Radial line reflections are controlled by specifying a maximum radial line length such that the reflection width can be neglected.

Finally, short line reflections may be added in place of long line reflections, but as mentioned earlier, the widths are narrow enough such that they cannot pass through the circuit.

CONCLUSION

In the Series 1600 system, all noise generation calculations were made with the parameters at their worst-case values or where possible by distributing them normally over their range and taking the 99.98% confidence level as an operating point.

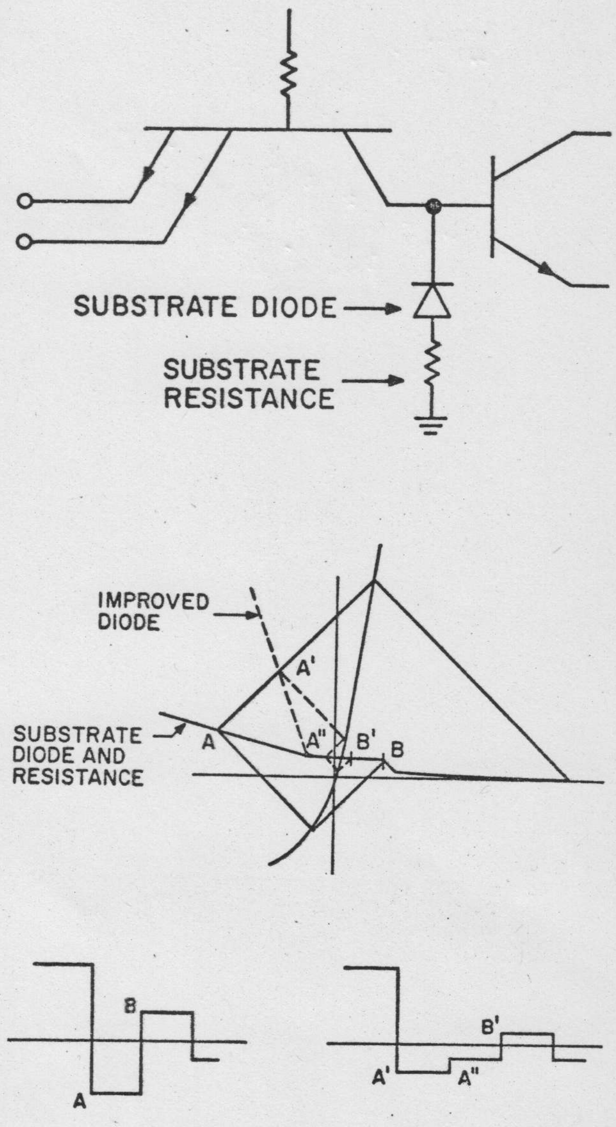


Fig. 13 End-of-line reflections were eliminated in series 1600 TTL circuits by improving the characteristics of the substrate diode.

The rules that evolved from this approach were implemented by a design automation program. This program has the capability of testing and correcting for all reflection wiring rules and testing for parallelism rules. It was found that approximately 83% of transmission lines in the system basic processor fell into the short-line category leaving only 17% which had to follow minimum spacing, radial line and cluster rules.

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